



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/920,390	07/31/2001	Meng-Jaw Cherng	JCLA4757-CIP	4405
7590	01/30/2004		EXAMINER	
J.C. PATENTS Suite 250 4 Venture Irvine, CA 92618			MALDONADO, JULIO J	
			ART UNIT	PAPER NUMBER
			2823	

DATE MAILED: 01/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/920,390

Applicant(s)

CHERNG ET AL.

Examiner

Julio J. Maldonado

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 03 November 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.  
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_ 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Response to Arguments***

1. Applicant's arguments see page 8, filed 11/03/2003, with respect to the rejection(s) of claim(s) 1-19 under 35 U.S.C. §103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Jang et al. (6,200,875 B1) in view of Jeong (U.S. 5,960,310) and Jost et al. (U.S. 5,605,857).

### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jang et al. (6,200,875 B1) in view of Jeong (U.S. 5,960,310) and Jost et al. (U.S. 5,605,857).

In reference to claims 1, 6, 12 and 15, Jang et al. (Figs.1-7) in a related method to form contact plugs (40) teach providing a semiconductor device having a first and second gates (20) over a substrate (10), wherein the said first and second gates (20) have sidewall spacers; forming a silicon oxide layer (30) over the semiconductor device; patterning the oxide layer (30) without planarizing it, to form a self-aligned contact window (35) that exposes a surface of the substrate (10) between the said first and second gates (20), wherein a dimension of the contact window (35) at a top is greater

Art Unit: 2823

than a distance between the sidewall spacers of the first second gates (20); forming a polysilicon layer (38) over the dielectric layer (30) and filling the self-aligned contact window (35); removing a portion of the polysilicon layer (38) lying above the dielectric layer (30); and removing a portion of the dielectric layer (30) so that the contact plug (40) is formed inside the self-aligned contact window (35) (column 3, line 48 – column 5, line 27).

Jang et al. fail to teach forming a silicon nitride liner layer prior to deposit a dielectric layer and patterning the dielectric and liner layer without planarizing the dielectric layer to form a contact window. However, Jeong (Figs.4A-4G) in a related method to form contact plugs teaches forming a liner layer (77) prior to deposit a dielectric layer (79, 81) and patterning the dielectric (79, 81) and liner layer (77) without planarizing the dielectric layer (79, 81) to form a contact window (82), wherein said liner layer comprises silicon nitride (column 6, lines 22 – 65). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to form a dielectric liner layer followed by depositing a dielectric layer as taught by Jeong in the contact plug method of Yoon et al., since the liner layer can be used as a polishing stop, accurately ending the polishing step (column 1, lines 53-57).

The combined teachings of Jang et al. and Jeong fail to expressly teach using said silicon nitride liner layer as an etch stop and wherein the dielectric liner layer is converted into second sidewall spacers for the first gate and the second gate. However, Jost et al. (Figs.1-2) in a related method to form self-aligned contact plugs teach forming at least a first gate (12) and a second gate (14) over a substrate (11),

Art Unit: 2823

wherein said first (12) and second (14) gates have sidewall spacers (18); forming a dielectric liner layer (20) over said substrate (11) and said first (12) and second (14) gates, wherein said liner (20) comprises silicon nitride; forming a dielectric layer (28) over the liner layer (20); patterning the dielectric layer (28) using the dielectric liner layer (20) as an etch stop to form a self-aligned contact window (34) that exposes a surface of the substrate (11) between the said first (12) and second (14) gates, wherein a dimension of the contact window (34) at a top is greater than a distance between the sidewall spacers (18) of the first gate (12) and the second gate (14), and the dielectric liner layer (20) is converted into second sidewall spacers for the first gate (12) and the second gate (14) (column 3, lines 7 – 62). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Jang et al. and Jeong the teachings of Jost et al. to enable using the liner layer of Jang et al. and Jeong and further etching according to the teachings of Jost, thus obtaining the second sidewall spacers because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed liner formation step of Jang et al. and Jeong and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

In reference to claims 2-5, 7-11, 13, 14 and 16-19, Jang et al. in combination with Jeong and Jost et al. teach the dielectric liner layer comprising silicon nitride (see Jeong, column 6, lines 35-40); the dielectric layer comprising silicon oxide with a thickness of between 5,000Å to 10,000Å (Jang et al., column 3, lines 18 – 22), where

Art Unit: 2823

the dielectric layer comprises a dielectric layer with a good gap-filling capability and a dielectric passivation layer (Jeong, column 6, lines 41-65); and removing the portion of the polysilicon above the dielectric layer includes chemical-mechanical polishing (Jang et al., column 3, lines 47 – 56 and Jeong, column 7, lines 21 – 51). Jang et al. in combination with Jeong fail to teach the dielectric layer having a thickness of about 10,000Å to 15,000Å. Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

### ***Response to Arguments***

4. Applicant's arguments with respect to claims 1-19 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

6. Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist whose telephone number is (703) 308-0956 until 2/4/04. See MPEP 203.08.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner George Fourson whose telephone number is (703) 308-2544 until 2/4/04 and (571) 272-1860 thereafter. The examiner can normally be reached on Monday through Friday.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (703) 306-2794 until 2/4/04 and (571)

Art Unit: 2823

272-1855 thereafter. The fax number for this group is 703-872-9306 for before final submissions, 703-872-9306 for after final submissions and the customer service number for group 2800 is (703) 306-3329. Updates can be found at <http://www.uspto.gov/web/info/2800.htm>.

George Fourson  
Primary Examiner  
Art Unit 2823

Julio J. Maldonado  
January 20, 2004

  
G. Chen  
Supervisory Patent Examiner  
Technology Center 2800